AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): A semiconductor memory device comprising:

subword drivers (SWDs), each of which has a plurality of subword driver circuits commonly connected to a main word line and also connected to different subword selection lines to drive respective subword lines, each of the SWDs being connected to driver input terminals and the subword lines; and

a common inverter circuit having an inverter input terminal and an inverter output terminal, the inverter input terminal being connected to the main word line and the inverter output terminal being connected to the plurality of driver input terminals,

wherein each of the subword driver circuits includes an internal inverter circuit that is connected to an inverter output terminal connected to the main word line and the subword selection lines and has its output terminal connected to the subword lines, and a drive transistor connected to the subword selection lines, the inverter output terminal and the output terminal of the internal inverter circuit, and

each of the subword driver circuits is driven by a subword selection signal received through one of the subword selection lines.

2. (original): The semiconductor memory device according to Claim 1, wherein

the internal inverter circuit is constructed of a PMOS transistor and an NMOS transistor having their gates and drains commonly connected to the main word line, and

the source of the PMOS transistor is structured to the subword selection lines, and an output of the internal inverter is taken out from the commonly connected drains.

3. (original): The semiconductor memory device according to Claim 2, wherein the drive transistor is structured by an NMOS transistor having a drain connected to the subword selection lines, a source connected to the subword lines, and a gate connected to the output terminal of the common inverter circuit.

4. (original): The semiconductor memory device according to Claim 1, wherein the common inverter circuit is structured by two transistors.

5. (original): The semiconductor memory device according to Claim 4, wherein

the common inverter circuit and the main word line are shared by four subword driver circuits.

6-8. (canceled).

9. (new): The semiconductor memory device according to Claim 1, wherein said common inverter circuit is common to said plurality of subword driver circuits, and an occupied area in the semiconductor memory device is reduced.